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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,955	08/21/2006	Volker Harle	5367-220PUS	9357
27799 7590 11/06/2008 COHEN, PONTANI, LIEBERMAN & PAVANE LLP 551 FIFTH AVENUE SUITE 1210 NEW YORK, NY 10176				
EXAMINER CAMPBELL, SHAUN M				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/566,955

Applicant(s)

HARLE, VOLKER

Examiner

SHAUN CAMPBELL

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date _____

FINAL ACTION

1. Amendment A, received 8/18/2008, has been entered into the record.
2. Claims 1-15 are presented for examination. Claims 1-14 are currently amended and claim 15 is new.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because it contains over 150 words and because of the use of legal phraseology, for example "said mask material".

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-8 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haerle (US Patent No. 6,100,104) in view of Shi et al. (US Patent No. 5,693,962) hereafter referred to as Shi.

7. As to claim 1, Haerle discloses a method for the production of a plurality of optoelectronic semiconductor chips (a plurality of light emitting diode chips 100 as shown in figs 5-6) each having a plurality of structural elements with each structural element comprising at least one semiconductor layer (fig 5, layers 21, 22, and 23; col. 7, lines 1-5), comprising the steps of:

providing a chip composite base (fig 1-3 substrate wafer 19) having a substrate (fig 1-5, growth substrate wafer 3) and a growth surface (fig 1, the main surface 9)

forming on the growth surface a mask material layer (fig 1, mask layer 4) with a multiplicity of windows (fig 3, mask openings 10), wherein a mask material is chosen in such a way that a semiconductor material of the semiconductor layer that is to be grown in a later method step essentially cannot grow on said mask material or can grow in a substantially worse manner in comparison with the growth surface (col. 6, lines 55-67);

essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows (fig 4, the semiconductor layers themselves are the structural elements); and

singulating the chip composite base applied material to form semiconductor chips each having a plurality of structural elements (col. 7, lines 33-36; figs 5-6; the semiconductor layers themselves are the structural elements).

However, Haerle fails to disclose:

most of the windows have an average extent less than or equal to 1 micrometer.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Haerle, as evidenced by Shi.

Shi discloses a full color organic light emitting diode array comprising:

most of windows have an average extent less than or equal to 1 micrometer (col. 4, lines 15-27; col. 5, line 66 to col. 6 line 8; Examiner interprets the average extent being the depth of the windows).

Given the teaching of Shi, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Haerle by employing the well known or conventional feature of windows with an average extent less than or equal to 1 micrometer, such as disclosed by Shi, in order to produce a display with the desired size and resolution easily.

8. As to claims 2-8 and 12-15, Haerle discloses the method as claimed in claim 1 (paragraph above);

wherein the chip composite base (fig 1-3, substrate wafer 19) has at least one semiconductor layer grown epitaxially onto the substrate (col. 6, line 55 to col. 7, line 5) and the growth surface is a surface on that side of the epitaxially grown semiconductor layer (fig 4, the bottom side of 21 is in contact with the main surface 9) which is remote from the substrate (col. 6, lines 52-53)[claim 2].

wherein the chip composite base (fig 1-3, substrate wafer 19) has a semiconductor layer sequence grown epitaxially onto the substrate (col. 6, line 55 to col. 7, line 5) with an active zone that emits electromagnetic radiation (fig 4, light-emitting active layer 23), and the growth surface is a surface on that side of the semiconductor layer sequence (fig 4, the bottom side of 21 is in contact with the main surface 9) which is remote from the substrate (col. 6, lines 52-53)[claim 3].

wherein the structural elements respectfully have an epitaxially grown semiconductor layer sequence (col. 6, line 55 to col. 7, line 5) with an active zone that emits electromagnetic radiation (fig 4, light-emitting active layer 23)[claim 4].

wherein the mask material has SiO₂ or Al₂O₃ (col. 6, lines 38-39)[claim 5].

wherein, after the growth of the semiconductor layers (fig 5 is performed after fig 4), a layer made of electrically conductive contact material that is transmissive (front-side contact metallization layer 15, fig 5; it is transmissive because it would either bounce the radiation when a non-transparent material is used or pass the radiation through when a transparent material is used) to an electromagnetic radiation emitted by the active zone (fig 4, light-emitting active layer 23) is applied to the semiconductor layers, so that semiconductor layers of a plurality of structural elements are electrically

conductively connected to one another by the contact material (front-side contact metallization layer 15)[claims 6 and 15].

wherein the average thickness of the mask material layer (fig 9, mask layer 4) is less than the cumulated thickness of the semiconductor layers of a structural element (fig 9, semiconductor layer sequence 18)[claim 7].

wherein the mask material layer is at least partly removed after the growth of the semiconductor layers (col. 7, lines 13-20)[claim 8].

wherein the growth conditions for the growth of the semiconductor layers are at least one of set and varied during growth in such a way that semiconductor layers of the structural elements form a lens-shaped form, a truncated cone-shaped form, or a polyhedral form (col. 7, lines 66-67)[claim 12].

wherein the semiconductor layers are grown by means of metal organic vapor phase epitaxy (col. 6, lines 55-67)[claim 13].

an optoelectronic semiconductor chip, characterized in that it is produced according to a method as claimed in claim 1 (col. 7, lines 33-36)[claim 14]

9. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haerle in view of Shi as applied to claim 1, and further in view of Braun (US Patent No. 6,110,277).

10. As to claims 9-11, Haerle in view of Shi discloses the method as claimed in claim 1 (paragraphs above).

Haerle in view of Shi does not explicitly disclose
wherein, after the growth of the semiconductor layers, a planarization layer is applied over the growth surface [claim 9];
wherein a material whose refractive index is lower than that of the semiconductor layers is chosen for the planarization layer [claim 10]; or
wherein a dielectric material is chosen for the planarization layer [claim 11].

Nonetheless, these features are well known in the art and would have been an obvious modification of the method disclosed by Haerle in view of Shi, as evidenced by Braun.

Braun discloses wherein, after the growth of the semiconductor layers, a planarization layer is applied over the growth surface (fig 5, passivation layer 60)[claim 9] to protect the light-emitting diode;

wherein a material whose refractive index is lower than that of the semiconductor layers is chosen for the planarization layer (fig 5, the passivation layer 60 must have a refractive index that is lower than the semiconductor layers to allow the radiation to pass through, otherwise the radiation is blocked and the light-emitting diode could not shine)[claim 10]; and

wherein a dielectric material is chosen for the planarization layer (any material has dielectric properties, including the passivation layer 60)[claim 11].

Given the teaching of Braun, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Haerle in view of Shi by employing the well known or conventional features of

a lower refractive index planarization layer, such as disclosed by Braun, in order to make a light-emitting diode with good efficiency and optimized green, blue, and violet spectral region.

Response to Arguments

11. Applicant's arguments filed 8/18/2008 have been fully considered but they are not persuasive.

12. The Applicant argued in substance that nothing in Haerle teaches or suggests that the deposited semiconductor layers form structural elements of the resulting semiconductor bodies, or that the resulting chips include a plurality of structural elements each comprising at least one semiconductor layer as recited in claim 1.

13. Examiner respectfully traverses this argument because as described on page 8, lines 15-28 of the Applicant's specification the semiconductor layer sequence forms the structural elements. Therefore the semiconductor layers disclosed by Haerle also form structural elements.

14. In response to applicant's argument that Haerle is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention.

See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the prior art reference is in the field of applicant's endeavor.

15. The Applicant argued in substance that the cited passages of Shi refer to the depth of cavity structure 112, not to an average of its lateral dimensions.

16. Examiner respectfully traverses this argument because the claim does not state that the extent is an average of its lateral dimensions, and one interpretation of the structure as claimed includes interpreting the extent as being the depth of the windows.

17. In response to applicant's argument that Shi is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the prior art reference is in the field of applicant's endeavor and further the same types of problems having to do with the complications caused by the need of wet and dry etching and the fabrication of layers of different types of materials is the same for both organic and inorganic components.

Conclusion

Prior art made of record but not relied upon for this rejection is:

Linthicum et al. (US Patent No. 6,255,198 B2) Linthicum et al. teaches forming microelectronic structures including optoelectronic structures in windows having a size of around 3 micrometers.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **SHAUN CAMPBELL** whose telephone number is (571)270-3830. The examiner can normally be reached on **Monday Through Friday 8:00AM-5:30PM EST**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Ha can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shaun Campbell/
Examiner, Art Unit 2829
11/5/2008

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829